MMICs For Sensor Applications

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1. Abstract

A set of three commercial MMICs in coplanar environment have been developed, realized and tested successfully as cost effective basis for application in 25 GHz sensors. The circuits are designed using a coplanar component library which has been developed at the IMST and was seamless integrated into a commercially available circuit design program (HP-EEsof LIBRA).

2. Introduction

Today, the market situation of microwave products is very much different from what it was only a few years ago. Instead of military applications, in which prices did not play a significant role, commercial microwave applications and therefore circuits have become more and more important. MMICs are a very economical solution when mass production is established. Coplanar line technique, compared to microstrip technique, leads to a further cost reduction since the necessary chip area and processing steps are reduced. To increase the number of applications that these chips may be used in, the circuits must be as universal as possible. As simulation tool HP-EEsof's LIBRA Series IV, with our in house CPW element library [1], was used. With these points in mind the following MMICs are presented. They consist of a 3-stage tunable oscillator with MESFETs, a 2-stage frequency times five multiplier and a 2-stage amplifier using HFETs. The complete bias networks are situated on all the three MMICs. Only one positive bias voltage is necessary as bias supply.

3. Technology

The MMICs are fabricated in a 0.5 micron MESFET- (oscillator) as well as in 0.25 micron HFET- (multiplier, amplifier) technology [2]. The MMICs are designed in coplanar line technique. Using the coplanar instead of the microstrip line design neither a via hole etching, nor a backside metallisation is necessary. After thinning, the wafer is diced into the individual chips. A hybrid assembly process completed with filters and some interconnections is used to put the MMICs together on a 25 mil alumina substrate. Beside the use of the coplanar library, nonlinear models for the MESFETs and HFETs were mandatory for the circuit design.

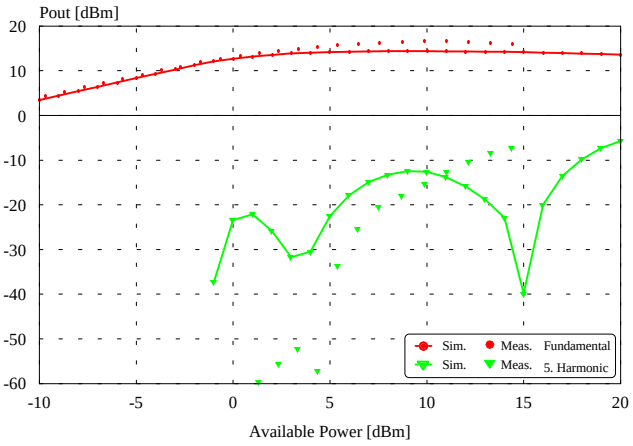

Fig.1: Measured and modeled output power of a HFET at f = 5.3 GHz, V_{DS} = 3 V and V_{GS} = 0 V.

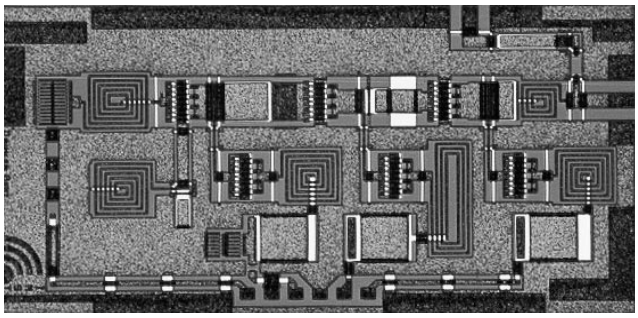

Fig. 2a: Photography of the tunable oscillator.

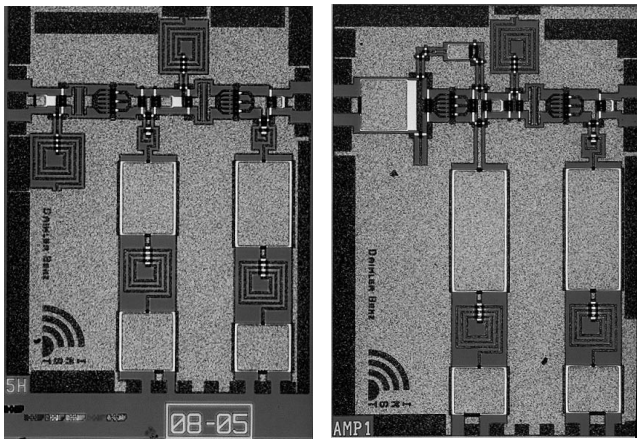

Fig. 2b: Photography of the times 5 multiplier (left) and the amplifier (right).

An example for such a model is shown in fig. 1 in case of the HFET used in the times five multiplier and the amplifier. While the accuracy of the modeled fundamental frequency output power is good, the 5th harmonic is reproduced with sufficient accuracy only around 10 dBm input power. This is due to the limited ability of the nonlinear transistor model to cope with higher harmonics.

4. MMICs

The oscillator is a 3-stage device (fig. 2a). While the first stage is the oscillator stage itself, the 2nd as well as the 3rd stage serve as a buffer. The oscillator is designed with serial feedback [3,4,5]. The 3-stage design was chosen for low frequency pulling due to load changes. Each stage consists of an active-load as bias supply. This reduces the possibility of low frequency oscillation. The bias pulling is suppressed by an internal bias supply for the first stage. For a monolithic integration including the tuning element two schottky diodes are connected in series. The chip area is 2.6 by 1.3 mm². The times five multiplier is a 2-stage device (fig. 2b left). The first stage multiplies the input signal. The 2nd stage serves as a buffer and bandpass filter. The resistors at the gates are needed for low frequency stability. The chip area is 1.2 by 1.5 mm², including bias networks. The amplifier is also a 2-stage device (fig. 2b right). The input, interstage as well as the output matching network is designed for the 24 GHz to 26 GHz range. The occupied chip area is 1.2 by 1.7 mm², again accommodating all bias elements.

5. Measurement results

The measurements were carried out by means of IMST's unique universal measurement stand. This equipment allows for on wafer s-parameter, nonlinear and load pull measurements and includes the characterization of frequency converting circuits [6]. The oscillator performance is shown in fig. 3. It works at 5 V bias supply. The output power is 11.6 ± 0.5 dBm over the required frequency range of 4.7 GHz to 5.3 GHz. The suppression of the 2nd and 3rd harmonic is better than 20 dB and 30 dB, respectively. The output return loss is lower than -15 dB. The output power of the 2nd output port is around -10 dBm and is necessary in connection with a frequency divider. The fre-

quency pulling caused by load mismatching of 6 dB return loss at the output port is better than 1 MHz. To reduce the bias pulling an internal voltage source for the first stage is applied, thus a frequency change of only 1 MHz / V is achieved.

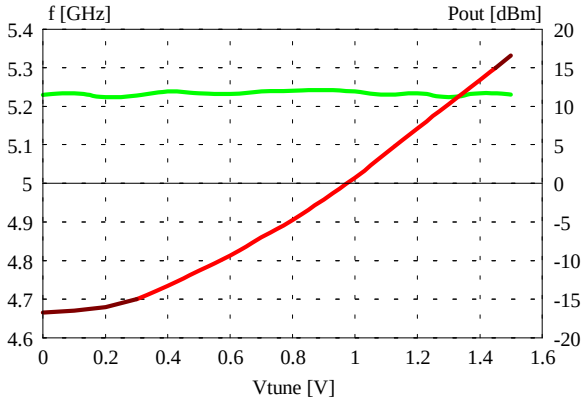

Fig. 3: Measured oscillator frequency and output power vs. tuning voltage.

By replacing the integrated tuning diode by an external varactor the frequency dependence from the tuning voltage becomes linear.

The performance of the times five multiplier is depicted in fig. 4. The output power of the 5th harmonic vs. the available input power of the fundamental frequency for the frequencies 4.7 GHz, 5.0 GHz and 5.3 GHz is shown. There is a good agreement between the measurement results and the simulated values around 10 dBm input power. In general, it is very difficult to model a transistor including the 5th harmonic generation! The conversion loss at 10 dBm input power (which is the oscillator output power) is around 12 dB. The input and output return loss is lower than -5 dB and -15 dB respectively. The large signal behavior of the following amplifier can be seen in fig. 5. It exhibits an amplification of approximately 15 dB. For an input power of -2 dBm (from the multiplier) an output power of 13 dBm was achieved. This is in very well agreement with the simulated data.

The simulated value of the saturated output power is 15 dBm, the measured value is around

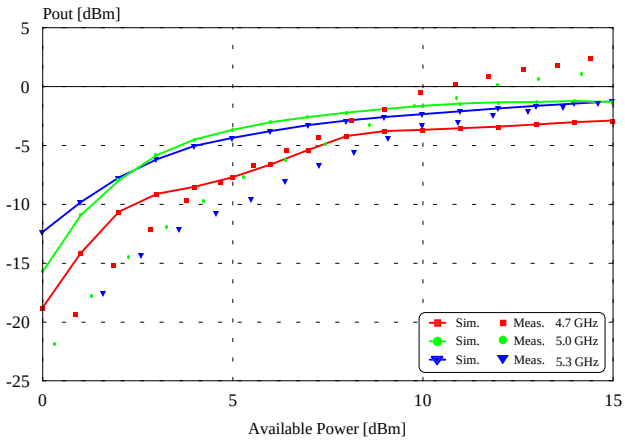

Fig. 4: Measured and simulated output power of the 5th harmonic vs. input power.

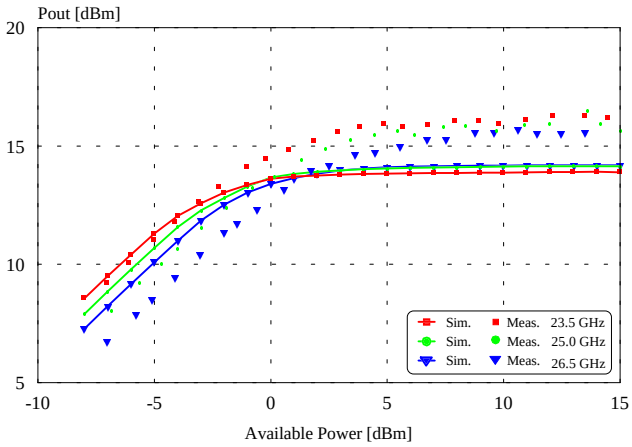

Fig. 5: Measured and simulated output power of the amplifier.

17 dBm, all for 3 V bias voltage. This difference is due to a higher than expected saturation current of the HFETs. The input as well as the output return loss is lower than -15 dB. The frequency conversion behavior of the complete system is shown in fig. 6. There is a suppression of more than 60 dB of the fundamental LO frequency and the overall conversion gain is around +1 dB. The minimum sideband suppression is 6 dB in case of the 4th harmonic and at

least 10 dB in case of the 6th harmonic.

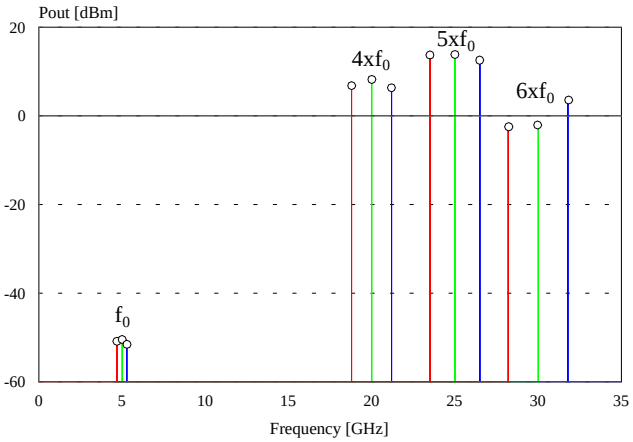

Fig. 6: Measured power spectrum of the complete sensor system. The utilized LO power is P_{LO} = 12 dBm.

6. Conclusions

An ensemble of three MMICs for sensor applications at 25 GHz was realized and tested successfully. Connecting these three MMICs, a tunable microwave source with 13 dBm output power was realized. All components are well designed by means of a complete simulation of all passive and active devices. Also the complete bias networks are situated on all the three MMICs. Only one positive bias voltage is necessary as bias supply.

7. References

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